In rejecting claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54 under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Rostoker and Liang, the Examiner acknowledges "[t]he admitted prior art fails to specify the semiconductor chip having two or more chip electrodes in a common wiring layer...". However, the Examiner takes the position that this missing teaching is found in Rostoker, stating: "Rostoker teaches using a semiconductor chip comprising a variety of internal connections and having an electrode set comprising two electrodes being connected to a common wiring layer...".

Actually, Rostoker teaches three variations: two external bump pads connected directly to the substrate material of the die (and not a wiring layer); two external bump pads each connected to one of two chip electrodes, which are in turn connected to a single wiring layer; and two external bump pads, only one of which is connected to a chip electrode, which is in turn connected to a single wiring layer (the two external bump pads are connected by an external surface connector called a "surface jumper"). (See Fig. 2b; col. 11, line 23 - col. 12, line 13). In other words, Rostoker teaches a plurality of raised bump contacts, but never only a single bump contact.

Neither Rostoker nor Lang teaches the combination of two chip electrodes connected to a single external bump pad, as required by the present claimed invention.. Moreover, this difference is more than merely academic as it provides Applicant with redundancy and improved reliability. Neither Rostoker nor Liang provides redundancy. In fact, Rostoker employs jumpered contacts as a means for solving routing problems in order to keep signal paths as short as possible (see col. 12, lines 14-17). Applicant's claimed invention, on the other hand, actually sacrifices area occupied by the chip electrodes by providing at least one chip electrode set comprising at least two chip electrodes, with a single external bump pad. Thus, Applicant's

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claimed invention, contrary to the general trend of reducing area, sacrifices area efficiency to obtain significantly improved reliability. (See the first full paragraph on page 8 of the specification.) That is to say, Applicant's claimed invention provides a single external bump pad with two chip electrodes, so that, should one of the electrodes fail, the electrical connection will still be intact. This solves an entirely different problem than those solved by the admitted prior art, Rostoker and Liang, and would not have been an obvious alteration to one skilled in the art.

Turning to the rejection of claims 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52 and 55 as obvious from the APA in view or Rostoker, Liang and further in view of Fulcher, and the rejection of claims 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53 and 56 as obvious from the APA in view of Rostoker, Liang and further in view of Fulcher and Bertolet et al., each of these claims also requires a single external bump pad electrically connected to two chip electrodes. The deficiencies of the APA combined with Rostoker and Liang vis-à-vis teaching or suggesting Applicant's claimed structure are discussed above. It is not seen that the secondary references Fulcher and/or Bertoloet et al. supply the missing teachings to the APA, Rostoker and Liang to achieve or render obvious any of the claims. It must be remembered the present invention bucks the trend of conventional wisdom of reducing area, and actually sacrifices area efficiency in order to obtain improved reliability. It is submitted one skilled in the art would not find Applicant's claimed invention obvious since it is counter to conventional trends and goals of reducing area.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

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The foregoing Amendment raises no new issues which require further search or consideration by the Examiner. Accordingly, entry of the foregoing Amendment, and allowance of the Application are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

Norman P. Soloway
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CERTIFICATE OF TRANSMISSION VIA FACSIMILE

I hereby certify that this correspondence is being sent via facsimile to EXAMINER NITIN PAREKH of the United States Patent and Trademark Office, facsimile number (703) 308-7722 on August 19, 2002 from Tucson, Arizona.

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MARKED COPY OF CLAIMS

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DOCKET: NEC N98039 CON

MARKED CLAIMS SHOWING CHANGES MADE

Please amend independent claims 21-23, 27-29, 33-35 and 39-41 to read as follows:

21. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

22. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

23. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

27. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring

layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external [pump] bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

28. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

29. (Twice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring

layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectivcly in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

33. (Twice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

34. (Twice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

35. (Twice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

39. (Twice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

40. (Twice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

41. (Twice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[an] a single external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.